REMARKS

I. Introduction

By the present Amendment, claim 2 has been amended. No claims have been added or canceled. Accordingly, claims 1-14 remain pending in the application. Claims 1, 6, and 11 are independent.

II. Office Action Summary

In the Office Action of September 20, 2005, claim 2 was rejected under 35 USC §112, second paragraph. Claims 1-14 were rejected under the judicially created doctrine of obviousness-type double patenting over claims 1-15 of U.S. Patent No. 6,611,107. Claims 1-14 were rejected under 35 USC §102(e) as being anticipated by U.S. Patent No. 6,509,692 issued to Komiya. These rejections are respectfully traversed.

III. Rejections under 35 USC §112

Claim 2 was rejected under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter regarded as the invention. Regarding this rejection, the Office Action indicates that claim 2 recites the limitation "said power supply control element." The Office Action notes, however, that there is no antecedent basis for this limitation in the claim.

By the present Amendment, Applicants have reviewed claim 2 and made appropriate amendments to address the issues of indefiniteness raised in the Office Action. It is therefore respectfully submitted that, as amended, claim 2 satisfies the requirements of 35 USC §112, second paragraph. Accordingly, withdrawal of this rejection is respectfully requested.

IV. Double Patenting Rejections

Claims 1-14 were rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-15 of the '107 patent.

Concurrently submitted herewith, is a Terminal Disclaimer that disclaims the terminal portion of any patents issued on the present application.

V. Rejections under 35 USC §102

Claims 1-14 were rejected under 35 USC §102(e) as being anticipated by Komiya. Regarding this rejection, the Office Action indicates that Komiya discloses an image display apparatus that comprises all of the features recited in the pending claims. With respect to independent claim 1, the Office Action alleges that the image display apparatus of Komiya includes a plurality of scanning wires, a plurality of signal wires, a plurality of current driven electro-optical display elements that are arranged in pixel regions surrounded by the scanning wires and the signal wires, and connected to a common power supply. The Office Action also indicates that Komiya discloses a plurality of driving elements arranged in the pixel region connected with the display elements. In particular, the Office Action alleges that Komiya discloses memory control circuits that sample and hold the signal voltage while blocking a bias voltage from being applied to each of the driving elements. Subsequently, the memory control circuit allegedly applies the held voltage to the driving elements as the bias voltage. Applicants respectfully disagree.

Independent claim 1 defines an image display apparatus that comprises:

> a plurality of scanning wires arranged in an image display region for transmitting a scanning signal;

a plurality of signal wires arranged to intersect with said plurality of scanning wires in said image display region for transmitting a signal voltage;

a plurality of current driven electro-optical display elements each arranged in a pixel region surrounded by said scanning wires and said signal wires connected to a common power supply;

a plurality of driving elements arranged in said pixel region connected with said electro-optical display elements; and

a plurality of memory control circuits for holding said signal voltage in response to said scanning signal to control driving of said driving elements based on said held signal voltage,

wherein said memory control circuit samples and holds said signal voltage while blocking a bias voltage from being applied to each of said driving elements, and subsequently applies said driving elements with said held signal voltage as said bias voltage.

According to independent claim 1, the image display apparatus comprises a plurality of scanning wires, a plurality of signal wires, a plurality of current driven electro-optical display elements, a plurality of driving elements, and a plurality of memory control circuits. The plurality of scanning lines are arranged in an image display region for transmitting a scanning signal, while the plurality of signal wires are arranged to intersect the scanning wires in the image display region for transmitting a signal voltage. The current driven electro-optical display elements are each arranged in a pixel region surrounded by the scanning wires, and signal wires and connected to a common power supply. The plurality of driving elements are also arranged in the pixel region and connected to the electro-optical display elements. The memory control circuits hold the signal voltage in response to the scanning signal in order to control driving of the driving elements based on the held signal voltage. According to independent claim 1, the memory control circuit samples and holds the signal voltage while blocking a bias voltage from being applied to each of the driving elements. Subsequently, the memory control circuit applies the signal voltage being held to the driving elements as the bias voltage. At least one benefit

achieved by the invention defined by independent claim 1 is that the display quality will not deteriorate even when there is a potential drop.

While the Office Action alleges that Komiya discloses the features of independent claim 1, Applicants' review of the cited passages has not revealed any specific disclosure for certain features recited in independent claim 1. In particular, Applicants note that Komiya does not appear to disclose a display device wherein the memory control circuits sample and hold the signal voltage while blocking a bias voltage from being applied. Komiya discloses a self-emissive display device that includes a selection TFT having a control gate connected to a gate line, and a drain connected to a data line. A driving TFT is also provided with a gate connected to a source of the selection TFT.

According to the display device of Komiya, the gate lines sequentially receive a gate signal that is applied by a gate line driver. The gate signal is a binary signal which is either an "ON" or "OFF" state. In the "ON" state, the signal has a predetermined positive voltage value. In the "OFF" state, the signal has a zero voltage value. When the gate signal of Komiya is turned on, TFTs of all the selection transistors connected to that gate are turned "ON", and the data line and the gate of the driving transistor are connected through the selection transistor. See Col. 1, lines 49-58. The driving transistor connects the driving line in the organic EL emissive element at an electrical conductivity corresponding to the value of the data signal. See Col. 1, lines 62-64. Accordingly, the memory retention capacitance and drive transistors are directly connected. This particular configuration prevents the bias voltage from being blocked. Komiya does not appear to provide any disclosure for claimed features such as "wherein said memory control circuit samples and holds said signal voltage while blocking a bias voltage from being applied to each of said

driving elements, and subsequently applies said driving elements with said held signal voltage as said bias voltage."

It is therefore respectfully submitted that independent claim 1 is allowable over the art of record.

Claims 2-5 depend from independent claim 1, and are therefore believed allowable for at least the reasons set forth above with respect to independent claim 1. In addition, these claims each introduce novel elements that independently render them patentable over the art of record.

Independent claim 6 defines an image display apparatus that comprises:

> a plurality of scanning wires arranged in an image display region for transmitting a scanning signal;
>
> a plurality of signal wires arranged to intersect with said plurality of scanning wires in said image display region for transmitting a signal voltage;
>
> a plurality of current driven electro-optical display elements arranged in a pixel region surrounded by said scanning wires and said signal wires connected to a common power supply;
>
> a plurality of driving elements arranged in said pixel region connected with said electro-optical display elements; and
>
> a plurality of memory control circuits for holding said signal voltage in response to said scanning signal to control driving of said driving elements based on said held signal voltage,
>
> wherein said memory control circuit samples and holds said signal voltage in said sampling period; and
>
> wherein a voltage applied to said driving elements in a sampling period is lower than a voltage in a write period.

According to independent claim 6, a plurality of scanning wires are arranged in an image display region for transmitting a scanning signal. A plurality of signal wires are also arranged to intersect with the scanning wires and to transmit a signal voltage. A plurality of current driven electro-optical display elements are arranged in pixel regions surrounded by the scanning wires and signal wires. The electro-optical

display elements are also connected to a common power supply. A plurality of driving elements are arranged in the pixel regions connected with the electro-optical display elements. A plurality of memory control circuits are provided for holding the signal voltage in response to the scanning signal in order to control the driving elements based on the signal voltage being held. According to independent claim 6, the memory control circuit samples and holds the signal voltage in the sampling period. Furthermore, the voltage applied to the driving elements during a sampling period is lower than the voltage applied during a write period.

The Office Action alleges that when the selection transistors are closed, the driving transistor is left opened so that a signal voltage from the data line is applied to the storage capacitor through the selection transistors. The Office Action alleges that this corresponds to a voltage being applied to the driving elements during a sampling period and alleges that no voltage is actually applied to the driving element. Review of Komiya, however, suggests that when the gate signal is turned on, the driving transistor connects to the driving line. Thus, voltage would necessarily be applied to the driving element. See column 1, lines 62-64.

The Office Action also alleges that Komiya further teaches that when the driving transistor is closed, the signal voltage held on the capacitor is applied to the driving transistor. This allegedly corresponds to the voltage signal being applied to the driving element during a write period. Further review of Komiya, however, appears to suggest that the particular passage cited by the Examiner is not truly a write period. Rather, according to Komiya, when the gate line driver selects another gate line, the data signal is stored by the storage capacitor for one vertical scanning period. During this time, the driving transistor maintains the electrical conductivity. However, the voltage has already been applied. This is only intended to maintain

the previously established electrical conductivity for one additional vertical scanning period while the gate line driver selects another gate. See column 2, lines 5-12. Komiya simply fails to disclose claimed features such as "wherein a voltage applied to said driving elements in a sampling period is lower than a voltage in a write period."

It is therefore respectfully submitted that independent claim 6 is allowable over the art of record.

Claims 7-10 depend from independent claim 6, and are therefore believed allowable for at least the reasons set forth above with respect to independent claim 6. In addition, these claims each introduce novel elements that independently render them patentable over the art of record.

Independent claim 11 defines an image display apparatus that comprises:

> a plurality of scanning wires arranged in an image display region for transmitting a scanning signal;
>
> a plurality of signal wires arranged to intersect with said plurality of scanning wires in said image display region for transmitting a signal voltage;
>
> a plurality of current driven electro-optical display elements arranged in a pixel region which is surrounded by said scanning wires and said signal wires connected to a common power supply;
>
> a plurality of driving elements arranged in said pixel region connected with said electro-optical display elements;
>
> a plurality of memory control circuits for holding said signal voltage in response to said scanning signal to control driving of said driving elements based on said held signal voltage;
>
> a power supply control element for controlling electric power supplied from said common power supply to said driving elements,
>
> wherein said memory control circuit samples and holds said signal voltage in said sampling period; and
>
> the electric power supplied to said driving elements in a sampling period is lower than the electric power in a write period.

Independent claim 11 recites features that are somewhat similar to those recited in independent claim 6. For example, independent claim 11 recites a feature that the electric power supplied to the driving elements in a sampling period is lower than the electric power supplied during a write period. As previously discussed with respect to independent claim 6, this particular feature is simply not disclosed by Komiya.

It is therefore respectfully submitted that independent claim 11 is allowable over the art of record.

Claims 12-14 depend from independent claim 11, and are therefore believed allowable for at least the reasons set forth above with respect to independent claim 11. In addition, these claims each introduce novel elements that independently render them patentable over the art of record.

VI. Conclusion

For the reasons stated above, it is respectfully submitted that all of the pending claims are now in condition for allowance. Therefore, the issuance of a Notice of Allowance is believed in order, and courteously solicited.

If the Examiner believes that there are any matters which can be resolved by way of either a personal or telephone interview, the Examiner is invited to contact Applicants' undersigned attorney at the number indicated below.

AUTHORIZATION

Applicants request any shortage or excess in fees in connection with the filing of this paper, including extension of time fees, and for which no other form of payment is offered, be charged or credited to Deposit Account No. 01-2135 (Case: 500.41297CX1).

Respectfully submitted,
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